

# Press Release

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## Leading ATE, EDA and Semiconductor Companies to Address Datalog Bottleneck in Yield Analysis

Standards Meeting to be Held July 17 in San Francisco During SEMICON West

**CUPERTINO, Calif., July 9, 2007** – The STDF Fail Data Standardization Group is holding an open meeting at SEMICON West on July 17 to review progress on the working group's effort to develop a standard format to enable easy sharing of structural fail information for manufacturing yield analysis. The Group, comprised of representatives from leading automatic test equipment (ATE) and electronic design automation (EDA) providers, along with several of the world's largest semiconductor manufacturers, was started after meetings initiated by Verigy beginning at SEMICON West in July 2006. It recently added IBM, Texas Instruments and Advantest to its growing list of participating companies. The Group is targeting initial internal test trials of the standard this fall, with a Beta site evaluation program planned for late 2007.

“As a group, we recognize that in order to identify yield-reducing failures, it is now necessary to standardize how failure data is transmitted between ATE and EDA tools,” said Group chairman, Ajay Khoche, who is Verigy's EDA/DFT alliance manager. “By working together, we will be able to fill a critical requirement that is emerging at 65nm and will only increase with each smaller process technology.”

“The impressive speed of the standardization process is further proof that there is a clear benefit for all the companies involved,” adds Andreas Leininger, Group vice-chairman and senior staff engineer, Test Resource Partitioning, Infineon Technologies. “The standard is important for reducing integration efforts of advanced test solutions in complex environments, and employing partnerships in design, manufacturing and test.”

At 65 nm process technologies and beyond, collecting and analyzing structural fail information in volume production is imperative for yield

improvements. Structural test techniques exist to collect the necessary data during manufacturing test. But to date, there has not been a widely-adopted, efficient standard format for storing and exchanging the structural fail data between test and design for yield analysis. The lack of a standard data storage format is further complicated by the fact that the typical semiconductor manufacturer uses design tools and test hardware from multiple vendors.

STDF is a well-established data format originally developed in 1993 by Teradyne for parametric failure data, and is still used for storing manufacturing test data for conventional yield analysis. It will provide a flexible starting point for the new standard, but needs further development to provide the efficient structural information required to analyze failures in deep sub-micron technology.

### **Open Invitation to the Industry**

Interested industry members who would like to participate in establishing this standard are invited to attend the group's meeting on Tuesday, July 17 from 2 to 4 p.m. PT at the Courtyard by Marriott, 299 Second Street in San Francisco. RSVP in advance to Ajay Khoche at +1 408.864.5123 or [ajay.khoche@verigy.com](mailto:ajay.khoche@verigy.com). More details are available here: <http://stdf.bcsweb.com/images/9/99/Invitation.pdf>.

### **STDF Fail Data Standardization Group Participating Companies**

The STDF Data Logging Standards Development Group is organized in two working groups to address the unique data logging requirements for logic and memory devices.

#### **Logic Device Working Group Members:**

Chair: Ajay Khoche, Verigy

Vice-Chair: Andreas Leininger, Infineon Technologies, AG

Participating Companies:

Advantest Corp.

BCS Consulting

Cadence Design Systems, Inc.

Credence Systems Corp.

Freescale Semiconductor

IBM

Infineon Technologies, AG

Inovys Corp.

Mentor Graphics Corp.

Open Source Consortium  
QUALCOMM Inc.  
Soto Technology  
STMicroelectronics  
Synopsys, Inc.  
Teradyne, Inc.  
Texas Instruments, Inc.  
Verigy  
Yield Dynamics, Inc.

**Memory Device Working Group Members:**

Chair: Ajay Khoche, Verigy  
Co-Vice-Chairs: Sauro Landini, ARM; Liyang Lai, Mentor Graphics Corp.  
Participating Companies:  
Mentor Graphics Corp.  
PDF Solutions, Inc.  
QUALCOMM Inc.  
Soto Technologies  
Teradyne, Inc.  
Verigy  
Virage Logic Corp.  
Yield Dynamics, Inc.

**STDF Fail Data Standardization Group**

The STDF Fail Data Standardization Group is an informal industry standards working group made up of representatives from automatic test equipment (ATE) suppliers, electronic design automation (EDA) tool vendors and leading semiconductor manufacturers to collaborate on a standard data format for sharing of structural fail information for yield analysis. The standard will benefit anyone who uses semiconductor test results and all interested parties are welcome to join the group. More information is available at <http://stdf.bcsweb.com>.